Study of 3D Integration Technology Based on Chip Transfer-Stacking for Heterogeneous Integrated Sensor System

	はしぐち ひ で と
氏　　名	橋 口 日 出 登
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指 導 教 員	東北大学教授　田中　徹
論 文 審 査 委 員	主査　東北大学教授　田中　徹　　東北大学教授　小野　崇人 東北大学教授　三浦　英生　　東北大学教授　寒川　誠二 東北大学准教授 福島　誉史

論 文 内 容 要 旨

3D integration technologies are promising approaches to overcome the interconnect-related problems of conventional LSIs. Using 3D integration technologies, various kinds of LSIs with various sizes, devices, and materials can be integrated into one chip, with TSVs. In addition, the structures of 3D stacked LSIs are suitable for parallel processing and multi-functional heterogeneous integration. A promising candidate, among 3D integration technologies, to achieve 3D integration with high production throughputs, high yields, and high flexibility in the sizes of stacked chips, is the chip transfer-stacking based MCtW 3D integration technology using self-assembly.

In Chapter 2, the chip transfer-stacking based MCtW 3D integration using self-assembly was demonstrated in the production of a heterogeneous integrated 3D sensor system, a 3D-RP chip. This chip is an electronic device to restore the visual perception of patients with age-related macular degeneration or retinitis pigmentosa, and is composed of an image sensor, a signal processing circuit layer, and a stimulus current generator circuit layer with stimulus current electrodes. These layers are electrically connected through TSVs, and integrated with 3D integration technologies. The photodiodes in the top layer convert incident light into electrical signals, these signals are delivered to the signal processing circuit in the next layer of the chip, and the stimulus current generator generates corresponding stimulus current pulses which will then stimulate the remaining retinal cells via a stimulus electrode array. Consequently, visual information is propagated to the brain, and patients can recognize light. The retinal prosthesis has several advantages: free eye movement, high resolution, and multiple functions such as visual information processing. Using MCtW 3D integration, 3D-RP chips with 37 × 37 pixels were successfully fabricated with electrical interconnects between the 1st photoreceptor and the base stimulus current generator chips, and their electrical properties were measured with the relation between light illuminance and stimulus current frequency. From there and the ensuing discussions concerning further developments of 3D-RP chips, a requirement emerged for 3D-RP chips with 138 × 138 pixels, capable of restoring visual perception to blindness patients with higher levels of QOL, a case for which the fabricated 37 × 37 pixels 3D-RP chips have insufficient resolution. In addition, the relations between pixel size and number of pixels were established, indicating that the pixel size, vertical interconnection pitch, TSV pad size, and bonding alignment accuracy were required to be smaller than what is feasible with conventional technologies. To achieve these smaller sizes and accuracy, three main serious issues in the conventional technologies of chip transfer-stacking based MCtW 3D integration using self-assembly were discussed. The first issue is misalignment of self-assembled chips due to external forces resulting from handling and temporary bonding processes. Because the self-assembled chips are only placed and not tightly fixed on carrier wafers, they are easily shifted by external forces resulting from handling processes (including temporary bonding); as a result, chips become misaligned. A maximum admissible acceleration of 3.2 m/s^2 was calculated, to ensure that the self-assembled chips remain fixed on the conventional carrier wafer; however, the maximum acceleration resulting from handling processes is approximately 5.1 m/s^2. The second issue is the inability of temporary adhesives to sustain high temperatures. Because of the low thermal stability of the temporary bonding/debonding systems used in MCtW 3D integration, the alignment accuracies of

the chips bonded to the support wafers with the adhesives are deteriorated by the thermal stresses applied during CVD processes. With CVD processes performed at 200 ℃, the chips suffered a maximum shift of approximately 7 μm. In addition, because of high process temperatures above 350 ℃, SA-CVD capable of uniformly depositing SiO_2 layers inside high aspect vias has not been adopted in the use of organic temporary adhesives for 3D integration using the typical via-last/back-side via TSV formation scheme. The third issue is difficulties in fine-pitch interconnect formation. In the MCtW 3D integration process, three-dimensionally stacked LSIs are electrically connected through microbump joints, and the microbump joining with a bonding pitch below 10 μm is still a challenging task because of the difficulties in injecting capillary underfill resins into small gaps between fine-pitch microbumps. To overcome these issues and attain target values for the production of 3D-RP chips with 138 × 138 pixels: 10-μm vertical interconnection pitch, 5-μm bonding alignment accuracy, and a 2-μm TSV size, three requirements were established: a method to fix self-assembled chips on carrier wafers, a highly thermoresistant temporary bonding/debonding system, and a fine-pitch interconnection method between the different stacked chip layers of 3D LSIs in MCtW.

In Chapter 3, SAE technology was proposed, as a viable method to increase the alignment accuracies of MCtW 3D integration based on transfer stacking. A fabrication process flow of bipolar SAE carriers was established, and SAE carriers were successfully fabricated. Applying DC voltages between the bipolar electrodes of the SAE carriers, self-assembled KGDs were electrostatically fixed on the carrier. The electrostatic adhesion force remains even after disconnecting their power sources. Using the fabricated SAE carriers, their KGD fixation properties were evaluated. This evaluation shows that the electrostatic adhesion strength increases gradually with the increase in applied voltage: the maximum adhesion strength was approximately 4 kPa at 500 V. Using this adhesion strength, the maximum admissible accelerations were calculated, for each applied voltage. The obtained results indicate that KGDs can be fixed on the SAE carrier and support the subsequent handling processes without detaching if the voltage applied to the bipolar electrodes is equal to (or greater than) 100 V, even if high acceleration linear stages with the maximum acceleration of 58.8 m/s^2 are used. The duration of the adhesion strengths of the self-assembled KGDs after disconnecting the power source was also evaluated, measuring the potential difference between the electrodes. This potential maintained approximately 90% of the initial value up until 15 min after power disconnection, if DC voltages of 200 V or above were applied to the bipolar electrodes, and approximately 81% of the electrostatic adhesion force was retained 15 min after disconnection of the power source. These KGD fixation properties suggest that the electrostatic adhesion is enough to temporarily fix KGDs on the SAE carriers and maintain high alignment accuracies obtained by self-assembly for at least 15 min after the DC voltage applied to the bipolar electrodes has been disconnected. In addition, the ESD damages caused by electrostatic fixation of self-assembled KGDs were evaluated with electric field simulations using FEM. The simulation results indicate that KGDs with silicon thicknesses beyond 10 μm can be electrostatically fixed on SAE carriers with applied voltage of 500 V or less without any ESD damage. Using the SAE carriers, a chip transfer-stacking based MCtW 3D integration using an SAE carrier was proposed and demonstrated, and nine KGDs with 1-μm thick Cu wirings and 10-μm high Cu/SnAg microbumps were processed through the via-last/back-side via 3D integration scheme, and Cu-TSVs and Cu/Sn microbumps were fabricated in KGDs thinned down to approximately 30 μm. The self-assembled KGDs were tightly fixed on the SAE carrier, and the KGDs were transferred to another support wafer, while keeping alignment accuracies within ± 5μm in both X and Y directions. These results show the feasibility of the chip transfer-stacking based MCtW 3D integration processes with self-assembled KGDs with high alignment accuracies. These high alignment accuracies can foster dramatic increases in the production yields of chip transfer-stacking based MCtW 3D integration approaches with fine-pitch and high-density microbump bonding.

In Chapter 4, combining SOG bonding with a-Si:H debonding using laser ablation, a new highly thermoresistant temporary bonding/debonding system was proposed and evaluated to support high temperature processes in chip transfer-stacking based MCtW 3D integration. Using the new system, a multichip SOG bonding process was demonstrated, and the shear bonding properties were evaluated by a bond tester. These results show that chips were successfully bonded to a quarts glass support wafer having a 100-nm thick a-Si:H layer. All the chips were tightly bonded to the support wafer with a shear bonding strength above 4 MPa. From the bonding strength measurement, the average shear bonding strengths of the chips with and without Cu wirings were determined to be 9.6 MPa and 8.7 MPa, respectively. It is noteworthy that the chips with the wirings could be tightly bonded to the glass wafer through the SOG. Therefore, the KGDs bonded to a a-Si:H layer deposited on glass support wafers through an SOG layer can endure harsh environment like grinding and the CMP processes used in typical MCtW 3D integration. Using the chips bonded on the support wafers, the chip debonding properties were also evaluated, irradiating the a-Si:H layer with a 248 nm KrF excimer pulse laser. With scan speeds in the range of 0.1–2.0 mm/sec, KGDs were successfully debonded from the support wafer by the laser irradiations with laser energy densities of (or above) 150 mJ/cm^2,

irrespective of the scan speeds. These evaluations suggest that the SOG and a-Si:H layers can be used for the highly thermoresistant temporary bonding/debonding systems. In addition, the chip transfer-stacking based MCtW 3D integration process using SAE carriers and SOG/a-Si:H temporary bonding/debonding technologies was experimentally demonstrated. In this advanced 3D integration approach, high temperature CVD processes were used for the formation of TSV liner dielectrics and passivation layers. The demonstration shows that the chips were accurately self-assembled on the SAE carrier, and the high-precision alignment was kept after TSV and the subsequent back side metallization processes. The KGD alignment errors caused by the high temperature CVD process the alignment errors were kept almost within ±1 μm. These results suggest that the proposed temporary bonding system can be adopted to chip-transfer stacking based MCtW 3D integration using SAE carriers with high-temperature CVD processes, above 350 ℃, keeping high alignment accuracy.

In Chapter 5, the MCtW direct bonding technology was discussed and proposed as a method to obtain fine-pitch interconnections in chip transfer-stacking based MCtW 3D integration using SAE carriers. To evaluate the effect on bonding strength of SiO_2 types and plasma sources for surface treatments, wafer-to-wafer direct bonding processes were demonstrated under several conditions, and their bonding strengths were evaluated by the crack opening method. The SiO_2 surfaces were treated by a plasma irradiation with Ar or N_2 and the subsequent water dipping. The obtained results show that the surface energies of the bonded wafers irradiated with N_2 plasma were slightly higher than that with Ar plasma. Therefore, N_2 plasma is more effective than Ar plasma to obtain high bonding qualities in oxide/oxide direct bonding processes. Using the surface treatment of N_2 plasma irradiation, simultaneous multichip-to-wafer direct bonding was demonstrated, and the bonding strengths were measured using thermal SiO_2 or PE-CVD SiO_2 with the plasma irradiation and the subsequent water dipping process. As a result, it was found that the average shear bonding strength between the thermal oxide wafers was 18.3 MPa, whereas the average strength between PE-CVD oxide wafers was 14.0 MPa. These results show that the shear bonding strengths between wafers/chips having a thermal oxide layer were higher than those having a PE-CVD oxide layer on one side or both sides. The results also show that the application of multichip-to-wafer direct oxide-oxide bonding technologies to transfer stacking based 3D integration using self-assembly is a promising technique. To investigate the effects of both N_2 plasma irradiation and water dipping processes on direct bonding strength, three types of surface treatment were performed on the surface of PE-CVD SiO_2 layers deposited on silicon wafers: water dipping, N_2 plasma activation, and both N_2 plasma activation and water dipping. The strongest average shear bonding strength was 19.5 MPa, for the N_2 plasma activation and water dipping condition. The conditions with only water dipping and with only N_2 plasma activation resulted in the also high average strengths of 13.1 MPa and 6.8 MPa, respectively. These results show that the wafer surface treatment with N_2 plasma irradiation and subsequent water dipping contributes to enhance the oxide/oxide direct bonding strengths. Additionally, to evaluate the bonding uniformity on the whole bonding area of the chips used in multichip-to-wafer direct bonding, a dicing test was performed to singulate the 5 mm^2 bonded chips into 1 mm^2 ones. The obtained results suggest that N_2 plasma irradiation both increases the bonding yields and strengthen multichip-to-wafer direct bonding between wafers with a CMP-treated PE-CVD oxide layer. To evaluate the relation between N_2 plasma irradiation and the water storage properties of the SiO_2 layers used for direct bonding, the amounts of H_2O content in the SiO_2 layers with/without N_2 plasma irradiation were measured with APIMS. The obtained results show that water storage in the SiO_2 surfaces is higher with N_2 plasma irradiation than without it, suggesting that the plasma treatment is effective to obtain the high water content surfaces. This is probably because the surface roughness is increased by the plasma treatment, thus creating larger SiO_2 surface areas, with the resulting increase in the amounts of surface water. It is also possible that nanovoids created by plasma irradiation contribute to the high water reservation property of the SiO_2 surfaces. These evaluations show that the proposed MCtW direct bonding technology using plasma-assisted direct bonding with N_2 plasma irradiation followed by water dipping has high potential for fine-pitch interconnect formation is chip transfer-stacking based MCtW 3D integration using self-assembly.

As a result of this work, chip transfer-stacking based MCtW 3D integration using self-assembly was successfully demonstrated for the production of heterogeneous integrated 3D sensor systems. To support the development of 3D sensor systems with smaller pixels and higher pixel densities than those achievable with conventional technologies, three new technologies for MCtW 3D integration were proposed and evaluated. Using the MCtW 3D integration based on the new technologies, heterogeneous integrated 3D sensor systems with higher performances than the conventional one can be produced.

論文審査結果の要旨

半導体集積回路(LSI)の飛躍的な進歩は，超高速大容量通信技術と結びついて今日の高度情報化社会をもたらした。今後もその進展は止まることなく続き，LSIと多種多様なセンサが協調した膨大なネットワークを構築し，時時刻刻生み出されるビッグデータが人々の生活を変えていく。これまでのLSIでは，微細化を唯一の指針として大規模化・高密度化・高性能化がなされてきたが，微細化の物理的・経済的な限界が確実に近づいている。また，従来の平面に構成された素子とそれを接続する長い水平配線による逐次信号処理がボトルネックとなり，高性能化が阻害されている。このような中，三次元集積化技術によってチップ間を最短の垂直配線で接続して高速かつ超並列信号処理可能なLSIを実現するとともに，機能の異なる複数のチップを積層して多機能と高機能を両立できる次世代の異種センサ集積システムが新しい価値を創造していくことになる。この異種センサ集積システムを実現するためには，多種多様な構造と機能を有するチップ群を，所定の位置に正確に配置して積層することが必要である。本論文は，下層のウェハやチップにかかる機械的負荷や熱的負荷を低減し位置合わせ精度を向上させる転写積層方式による三次元集積化技術についての研究したもので，全編6章からなる。

第1章は序論であり，本研究の背景，目的および構成を述べている。

第2章では，既存の転写積層方式を用いて受光回路チップと刺激電流生成回路チップを積層した37×37ピクセルの三次元積層人工網膜チップを世界で初めて作製することに成功し，基本動作である照度依存刺激電流生成とエッジ強調の有効性を実証している。また，人の顔をより詳細に識別できる138×138ピクセルを有する高解像度の三次元積層人工網膜チップのプロセス設計指針を明らかにしている。将来の異種センサを高集積化したシステムを作製するため，チップ積層における位置合わせの高精度化と垂直配線の微細化に着目して現状の転写積層方式の課題を明確にし，この課題を解決するチップ群の仮接合技術の有用性について述べており，工学的に重要な知見である。

第3章では，液体の表面張力を駆動力とする自己組織化実装により達成した高い位置合わせ精度を保持してチップ群を積層するために，チップを自己組織化実装する親疎水領域とチップ静電吸着可能なバイポーラ型櫛歯電極を有するキャリアウェハを提案し，試作によりその有効性を実証している。さらに，高解像度の三次元積層人工網膜チップを作製するのに十分な5μm以内の位置合わせ精度でチップ群を一括転写することに成功し，チップの薄化及び垂直配線の形成と電気的導通を確認している。本研究成果は，異種センサ集積システムの集積度と生産性を高めるために必須のチップ群高精度位置合わせと高スループット積層を両立する技術を確立したものであり，実用化に向けた有用な成果である。

第4章では，現行の転写積層方式で使用されている有機系接着剤を用いた仮接合技術の耐熱性を高め，チップ群の位置合わせ精度の向上による垂直配線の微細化を図るため，無機系接着剤を用いた高耐熱仮接合技術を提案し，試作による実証を行っている。スピンオングラスによる接着層と水素化アモルファスシリコンによる剥離層から成る積層膜を用いた新しい仮接合技術により，350℃以上の高温でも1□m以下の位置合わせ精度を保持し，直径2□m以下の微細な垂直配線を形成するために必要な準常圧熱CVDによる絶縁膜堆積が可能であることを実験的に確認している。垂直配線の電気的導通も確認できており，本研究成果は多種多様なチップ群を転写積層方式で一括集積するための基盤技術を確立したものであり，工学上重要な成果である。

第5章では，垂直配線の微細化と狭ピッチ化の問題を解決するため，酸化膜を介したプラズマ活性化直接接合によりバンプレスで多数のチップをウェハに一括接合して転写積層する技術を提案し，試作によりその有効性を実証している。また，接合面の表面吸着水が接合強度に与える影響を評価し，直接接合のメカニズム解明に資する重要な結果を示している。さらに，厚さの異なるチップの接合収率を高めるために緩衝層を介して一括接合することに成功している。これらの成果はバンプレスで垂直配線の微細化と狭ピッチ化ができる基盤技術を確立したものであり，工学上重要な成果である。

第6章は結論である。

以上要するに，本論文は，次世代の異種センサ集積システムを実現するために不可欠なマルチチップ一括転写積層技術の開発を目的に，1)高精度・高スループットの自己組織化静電吸着技術，2)微細な垂直配線を高収率で形成することが可能な高耐熱仮接合技術，3)チップ一括直接接合技術の開発に成功したもので，三次元集積化技術の実用化を大きく推進する成果であり，バイオロボティクスおよび半導体集積回路工学の発展に寄与するところが少なくない。

よって，本論文は博士(工学)の学位論文として合格と認める。